EAST SEARCH

9/20/03

L#	Hits	Search String	Databases
L2	132	(mutually same exclusive same operations) same parallel$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Results of search set L2:

WO 9944122 A2	A METHOD FOR STRUCTURING A MULTI-INSTRUCTION COMPUTER PROGRAM	19990902	
US 6616354 B2	Method and apparatus for adjusting printhead to print-media travel path spacing in a printer	20030909	400/56
US 6587942 B1	Circuit for converting input serial data in a plurality of possible formats into output data in parallel format by interpreting input data format indication information	20030701	713/100
US 6584589 B1	Self-testing of magneto-resistive memory arrays	20030624	714/721
US 6581187 B2	Automatic design of VLIW processors	20030617	716/1
US 6557049 B1	Programmable computerize enclosure module for accommodating SCSI devices and associated method of configuring operation features thereof	20030429	710/8
US 6529989 B1	Intelligent expansion ROM sharing bus subsystem	20030304	710/306
US 6504745 B2	High performance erasable programmable read-only memory (EPROM) devices with multiple dimension first-level bit lines	20030107	365/63
US 6457173 B1	Automatic design of VLIW instruction formats	20020924	717/149
US 6408428 B1	Automated design of processor systems using feedback from internal measurements of candidate systems	20020618	716/17
US 6404670 B2	Multiple ports memory-cell structure	20020611	365/154
US 6385757 B1	Auto design of VLIW processors	20020507	716/1
US 6343045 B1	Methods to reduce the effects of leakage current for dynamic circuit elements	20020129	365/227
US 6289434 B1	Apparatus and method of implementing systems on silicon using dynamic-adaptive run-time reconfigurable circuits for processing multiple, independent data and control streams of varying rates	20010911	712/32
US 6282708 B1	Method and processor for structuring a multi-instruction computer program in an internal directed acyclic graph	20010828	717/156
US 6237046 B1	Input/output control apparatus managing cache memory utilizing a spare hash table for operations if first hash table enters a synonym state	20010522	710/1

US 6178463 B1	Object-oriented data processing system with transactional adapter	20010123	709/315
US 6175914 B1	Processor including a combined parallel debug and trace port and a serial port	20010116	712/227
US 6175914 B	Processor has parallel debug port enabled through serial debug port and operated synchronously with the clock provided to the serial debug port in a mutually exclusive manner with the operation of the trace port	20010116	
US 6144228 A	Generalized push-pull cascode logic technique	20001107	326/121
US 6134173 A	Programmable logic array integrated circuits	20001017	365/230.03
US 6108229 A	High performance embedded semiconductor memory device with multiple dimension first-level bit-lines	20000822	365/52
US 6098112 A	Streams function registering	20000801	709/321
US 6064599 A	Programmable logic array integrated circuits	20000516	365/189.01
US 6049861 A	Locating and sampling of data in parallel processing systems	20000411	712/28
US 6038651 A	SMP clusters with remote resource managers for distributing work to other clusters while reducing bus traffic to a minimum	20000314	712/21
US 6028808 A	Programmable logic array integrated circuits	20000222	365/230.03
US 6023439 A	Programmable logic array integrated circuits	20000208	365/230.03
US 6018490 A	Programmable logic array integrated circuits	20000125	365/230.03
US 6002687 A	MPEG transport stream remultiplexer	19991214	370/394
US 5963621 A	Secure communication system	19991005	379/93.08
US 5953515 A	Pluggable electronic card presence detect scheme for use in parallel and serial vital detect product data (VPD) collection systems	19990914	710/16
US 5926036 A	Programmable logic array circuits comprising look up table implementation of fast carry adders and counters	19990720	326/40
US 5892698 A	2's complement floating-point multiply accumulate unit	19990406	708/501
US 5892507 A	Computer system for authoring a multimedia composition using a visual representation of the multimedia composition	19990406	715/500.1
US 5883850 A	Programmable logic array integrated circuits	19990316	365/230.03
US 5874841 A	Sample-and-hold circuit for a switched-mode power supply	19990223	327/94
US 5869982 A	Programmable input-output cell with data conversion capability for programmable logic device	19990209	
US 5861738 A	DC to DC converter with a single-fault tolerant clamp	19990119	323/282
US 5848005 A	Programmable logic array integrated circuits	19981208	365/230.03
US 5838628 A	Programmable logic array integrated circuits	19981117	365/230.03
US 5835493 A	MPEG transport stream remultiplexer	19981110	370/395.62
US 5828229 A	Programmable logic array integrated circuits	19981027	326/40
US 5825704 A	High performance embedded semiconductor memory devices with multiple dimension first-level bit lines	19981020	365/222
US 5812479 A	Programmable logic array integrated circuits	19980922	365/230.03

US 5774698 A	Multi-media serial line switching adapter for parallel networks and heterogeneous and homologous computer system	19980630	712/1
US 5764583 A	Programmable logic array integrated circuits	19980609	365/230.03
US 5761531 A	Input/output control apparatus and method for transfering track data from cache module to channel unit during the staging of the data track from device adapter	19980602	710/21
US 5724414 A	Secure communication system	19980303	379/100.17
US 5691984 A	Compact, adaptable brouting switch	19971125	370/401
US 5668771 A	Programmable logic array integrated circuits	19970916	365/230.03
US 5651040 A	Dynamic division system and method for improving testability of a counter	19970722	377/29
US 5627827 A	Automatic service cutover for ISDN private exchange	19970506	370/359
US 5619722 A	Addressable communication port expander	19970408	710/2
US 5612953 A	Multi-media serial line switching adapter for parallel networks and heterogeneous and homologous computer systems	19970318	370/367
US 5576601 A	Drive circuit for electroluminescent panels and the like	19961119	315/169.3
US 5550782 A	Programmable logic array integrated circuits	19960827	365/230.03
US 5535373 A	Protocol-to-protocol translator for interfacing disparate serial network nodes to a common parallel switching network	19960709	703/25
US 5502771 A	Clock radio volume control appraratus	19960326	381/104
US 5502436 A	Method of identifying a signal path and signal processing apparatus	19960326	340/825.25
US 5495618 A	System for augmenting two dimensional data sets in a two dimensional parallel computer system	19960227	712/16
US 5487159 A	System for processing shift, mask, and merge operations in one instruction	19960123	712/223
US 5485103 A	Programmable logic array with local and global conductors	19960116	326/41
US 5479166 A	Huffman decoding method, circuit and system employing conditional subtraction for conversion of negative numbers	19951226	341/65
US 5471593 A	Computer processor with an efficient means of executing many instructions simultaneously	19951128	712/235
US 5436575 A	Programmable logic array integrated circuits	19950725	326/40
US 5412767 A	Image processing system utilizing brush profile	19950502	345/639
US 5412452 A	Apparatus and method for controlling diagnostic routines concurrently in a printing system	19950502	399/11
US 5404394 A	Secure communication system	19950404	379/100.12
US 5397475 A	Purification of hydrogen peroxide	19950314	210/661
US 5395076 A	Spacecraft velocity change maneuvers by variable arcjets	19950307	244/169
US 5376844 A	Programmable logic device with multiplexer-based programmable interconnections	19941227	326/41
US 5345146 A	Drive circuit for electroluminescent panels and the like	19940906	315/169.3
US 5318593 A	Multi-mode adaptable implantable pacemaker	19940607	607/9

US 5260610 A	Programmable logic element interconnections for programmable logic array integrated circuits	19931109	326/41
US 5203425 A	Personnel lift devices	19930420	182/19
US 5196761 A	Color cathode-ray tube	19930323	313/402
US 5161171 A	Digital data transmitting apparatus	19921103	375/357
US 5111074 A	Multi-input compound function complementary noise-immune logic	19920505	326/18
US 5013876 A	Switch contacts with improved fault-closing capability	19910507	200/254
US 4963860 A	Integrated matrix display circuitry	19901016	345/206
US 4958632 A	Adaptable, digital computer controlled cardiac pacemaker	19900925	607/11
US 4872002 A	Integrated matrix display circuitry	19891003	345/55
US 4705180 A	Suspended load positioning stabilizing system	19871110	212/307
US 4607176 A	Tally cell circuit	19860819	377/33
US 4585434 A	Top loading swinging bucket centrifuge rotor having knife edge pivots	19860429	494/20
US 4585433 A	Sample container for a top loading swinging bucket centrifuge rotor	19860429	494/20
US 4483088 A	Revolver empty chamber indicia	19841120	42/1.05
US 4342001 A	Differential amplifier having a low-pass characteristic	19820727	330/9
US 4255045 A	Removable light box	19810310	355/37
US 4190834 A	Circuit and method for producing a full-screen cross-hair cursor on a raster-scan type display	19800226	345/162
US 4096582 A	Field-accessed magnetic bubble mutually exclusive circuits with common elements	19780620	365/13
US 3965372 A	Signal transmission gate	19760622	327/482
US 3928772 A	Time dependent fault detector	19751223	307/116
US 3875568 A	Magnetic bubble circuit with hard-soft overlay	19750401	365/38
US 3866567 A	MASKING APPARATUS FOR USE IN COATING AN ARTICLE OF MANUFACTURE	19750218	118/69
US 3866090 A	GAS DISCHARGE PANEL AND OPERATING SYSTEM	19750211	345/67
US 3829596 A	SONAR REVERBERATION SIMULATOR	19740813	434/6
US 3814947 A	ELECTRICAL CIRCUIT FOR PROVIDING AUTOMATIC ALTERNATE SWITCHING	19740604	307/41
US 3800273 A	PORTABLE SONAR SYSTEM	19740326	367/105
US 3696780 A	APPARATUS FOR APPLYING POWERED COATING MATERIAL TO AN ARTICLE	19721010	118/69
US 3665152 A	IRON WITH OVERTEMPERATURE PROTECTION MEANS	19720523	219/253
US 3643243 A	MEMORY SYSTEM HAVING ASSOCIATED PLURAL TIMING TRACKS AND DATA TRACKS	19720215	360/63
US 3576368 A	IMAGING SYSTEM	19710427	355/51
US 20030172205 A1	Methods and components for mechanical computer	20030911	710/45
US 20030128052 A1	Programmable logic array integrated circuits	20030710	326/41

US 20030079625 A1	Method and apparatus for adjusting printhead to print-media travel path spacing in a printer	20030501	101/59
US 20030043657 A1	High performance embedded semiconductor memory devices with multiple dimension first-level bit-lines	20030306	365/200
US 20030040814 A1	Method for controlling mechanisms and technical systems a corresponding device and control software	20030227	700/42
US 20020194159 A1	Parallel object-oriented data mining system	20021219	707/2
US 20020133784 A1	Automatic design of VLIW processors	20020919	716/1
US 20020130681 A1	Programmable logic array integrated circuits	20020919	326/41
US 20020120914 A1	Automatic design of VLIW processors	20020829	716/17
US 20020039317 A1	High performance erasable programmable read-only memory (EPROM) devices with multiple dimension first-level bit lines	20020404	365/222
US 20010010654 A1	Multiple ports memory-cell structure	20010802	365/222
US 20010003513 A1	Methods to reduce the effects of leakage current for dynamic circuit elements	20010614	365/222
NNRD42298	Neuron Autonomous Logic Circuits	19990601	
NN9110154	Embedded Sequential Coding During Steady State Control Conditions.	19911001	
NN8907351	Tentative Edge Classification Using Truth Tables	19890701	
NN8607657	Hierarchical Organization in an Array Structure	19860701	
NN77122547	Variable I Fetch. December 1977.	19771201	
NN74053858	Precision Modulation Technique. May 1974.	19740501	
NN7308942	Test Access Arrangement for LSI Computers. August 1973.	19730801	
NB9309131	Efficient Evaluation of X**N for Lighting Calculations	19930901	
NB8909400	Ce Controlling Chip Scan Strings for Self-Test, LSSD and Debug Tests	19890901	
NA83123510	Clock Driver, Translator and Latch Circuit	19831201	
NA82123578	Data Base Control and Processing System. December 1982.	19821201	
NA81123130	Pageable Control Memory With Time Overlapped Output and Input Operations. December 1981.	19811201	
JP 2001101584 A	Vehicle traffic controlling system in roads, railway station, has stop configured to exclusive path of main line which diverts vehicles to up and down lane of other paths	20010413	
JP 09041518 A	WEB-VOID CLOSING METHOD OF PARTITION MOUNTING SECTION OF FLAT DECK PLATE	19970210	
EP 517429 A2	CPU with integrated multiply/accumulate unit.	19921209	
DE 2162988 B	Control unit for A.C. regulator - has control circuit which utilises two contact-less switching devices operated in a mutually exclusive cycling mode	19750213	